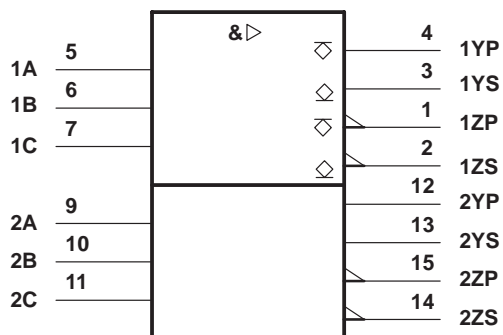


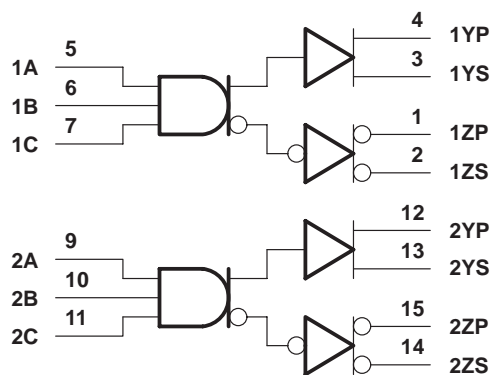
SN55114, SN75114 DUAL DIFFERENTIAL LINE DRIVERS

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logic symbol†



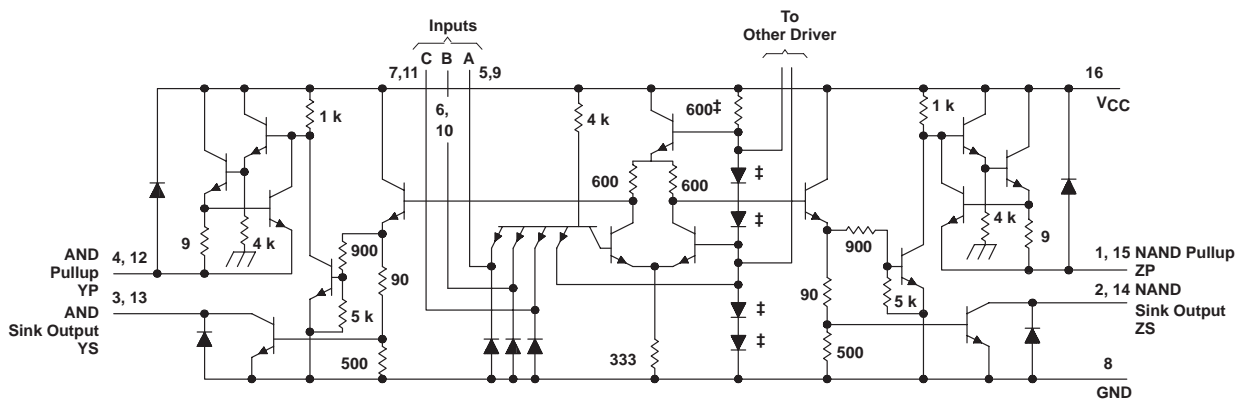
logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the D, J, N, and W packages.

schematic (each driver)



‡ These components are common to both drivers. Resistor values shown are nominal and in ohms.

Pin numbers shown are for the D, J, N, and W packages.

SN55114, SN75114 DUAL DIFFERENTIAL LINE DRIVERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J or W package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W‡	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK, J, and W packages, SN55114 chips are either silver glass or alloy mounted.

recommended operating conditions (unless otherwise noted)

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			–40			–40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	–55		125	0		70	°C



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN55114			SN75114			UNIT		
		MIN	TYP‡	MAX	MIN	TYP‡	MAX			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -12 mA	-0.9	-1.5		-0.9	-1.5		V		
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V	I _{OH} = -10 mA			2.4	3.4		2.4	3.4	V
		I _{OH} = -40 mA			2	3		2	3	
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 40 mA		0.2	0.4		0.2	0.45		V	
V _{OK} Output clamp voltage	V _{CC} = 5 V, I _O = 40 mA, T _A = 25°C		6.1	6.5		6.1	6.5		V	
	V _{CC} = MAX, I _O = -40 mA, T _A = 25°C		-1.1	-1.5		-1.1	-1.5			
I _{O(off)} Off-state open collector output current	V _{CC} = MAX	V _{OH} = 12 V	T _A = 25°C			1	100			μA
			T _A = 125°C				200			
		V _{OH} = 5.25 V	T _A = 25°C					1	100	
			T _A = 70°C						200	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1			1		mA	
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V			40			40		μA	
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V		-1.1	-1.6			-1.1	-1.6	mA	
I _{OS} Short-circuit output current§	V _{CC} = MAX, V _O = 0, T _A = 25°C	-40	-90	-120	-40	-90	-120		mA	
I _{CC} Supply current (both drivers)	All inputs at 0 V, No load, T _A = 25°C	V _{CC} = MAX			37	50		37	50	mA
		V _{CC} = 7 V			47	65		47	70	

† All parameters, with the exception of off-state open-collector output current, are measured with the active pullup connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.

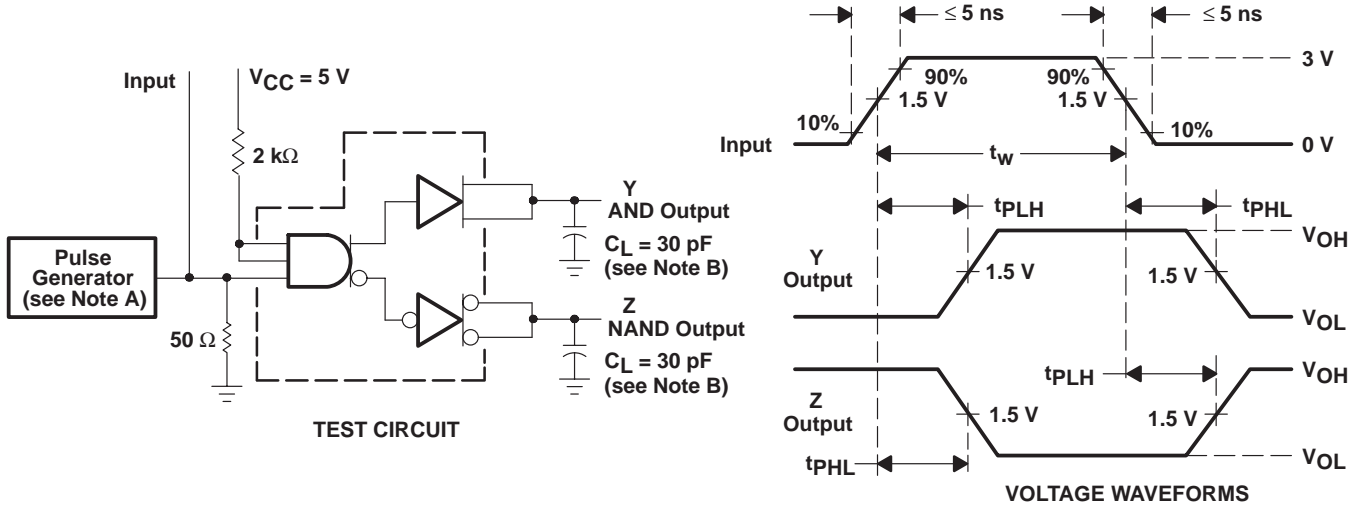
§ Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN55114			SN75114			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH} Propagation delay time, low- to high-level output	C _L = 30 pF, See Figure 1		15	20		15	30	ns
t _{PHL} Propagation delay time, high- to low-level output			11	20		11	30	ns



PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O = 500 \Omega$, $PRR \leq 500 \text{ kHz}$, $t_w \leq 100 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS†

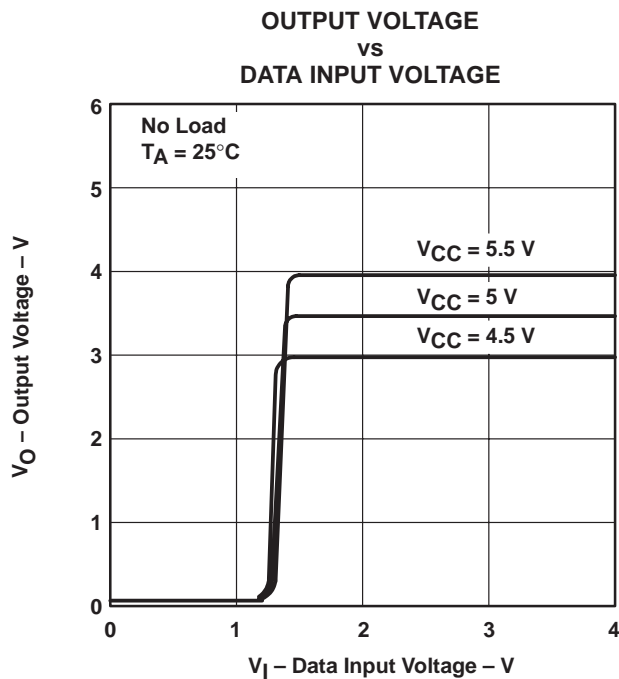


Figure 2

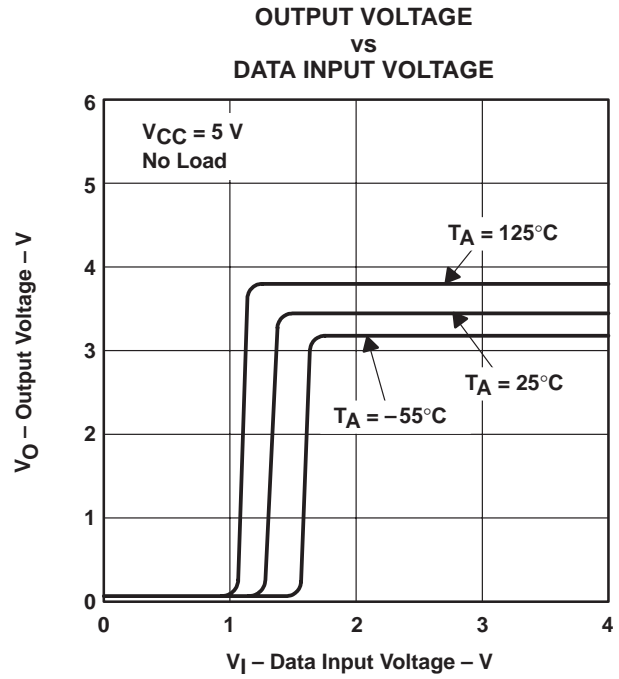


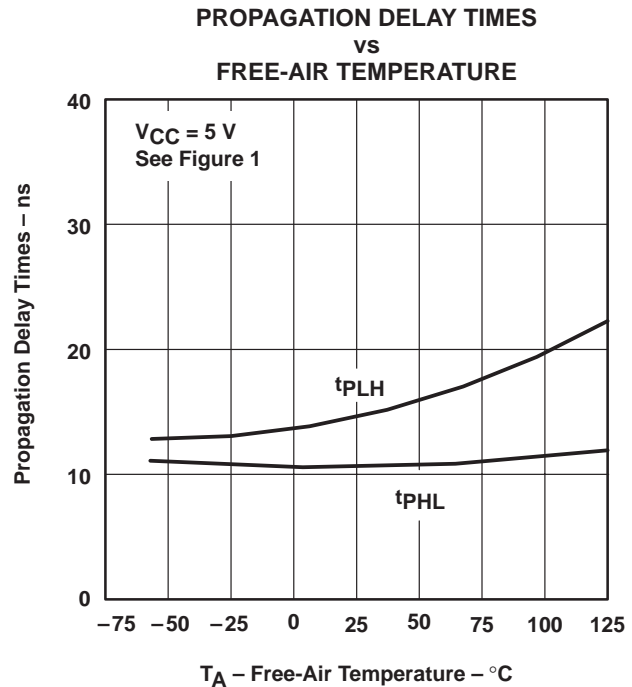
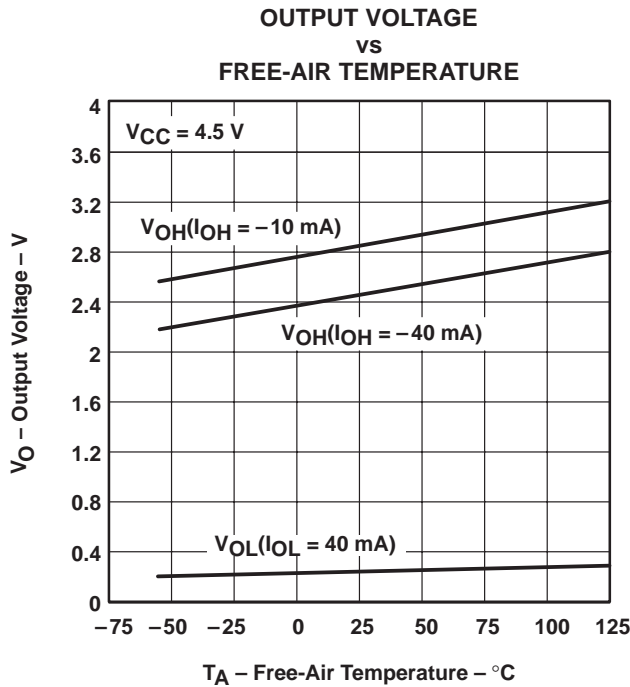
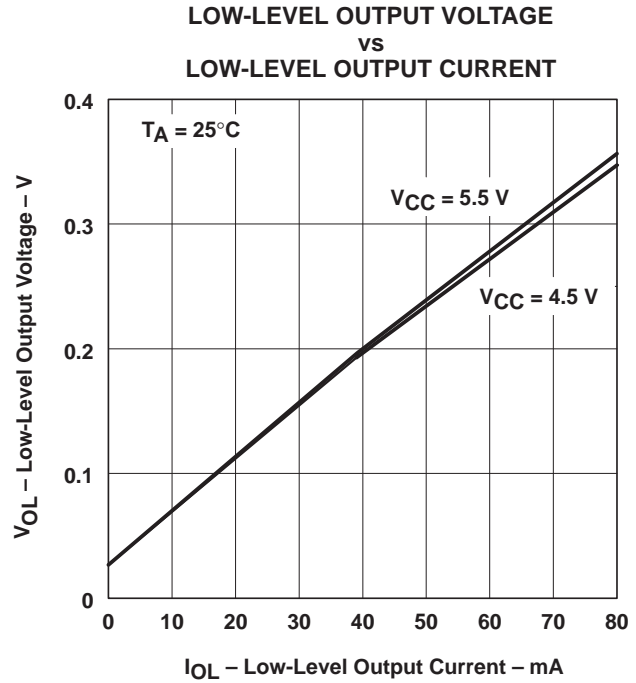
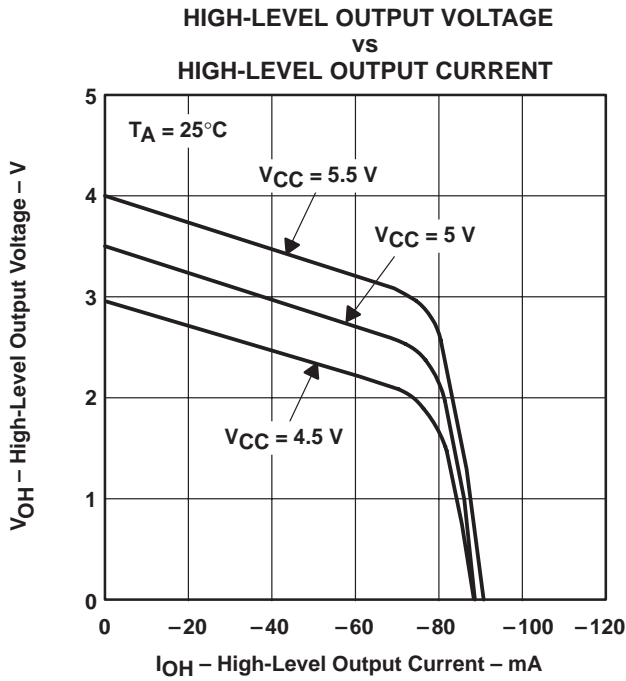
Figure 3

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.

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TYPICAL CHARACTERISTICS†



† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.

TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
 (BOTH DRIVERS)
 vs
 SUPPLY VOLTAGE

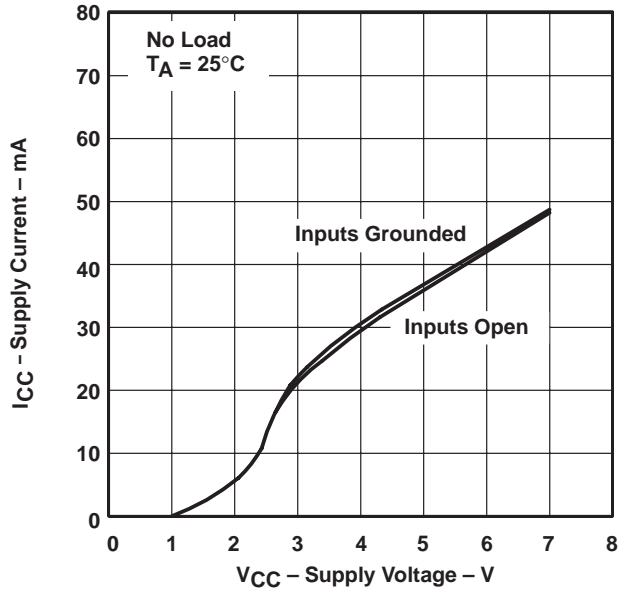


Figure 8

SUPPLY CURRENT
 (BOTH DRIVERS)
 vs
 FREE-AIR TEMPERATURE

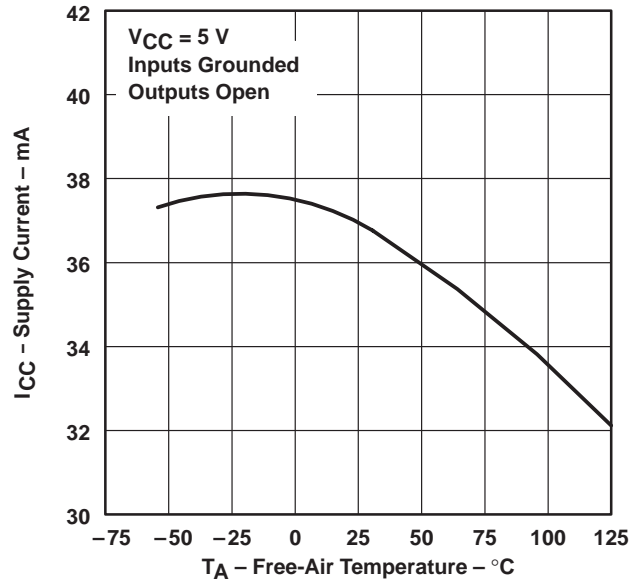


Figure 9

SUPPLY CURRENT
 (BOTH DRIVERS)
 vs
 FREQUENCY

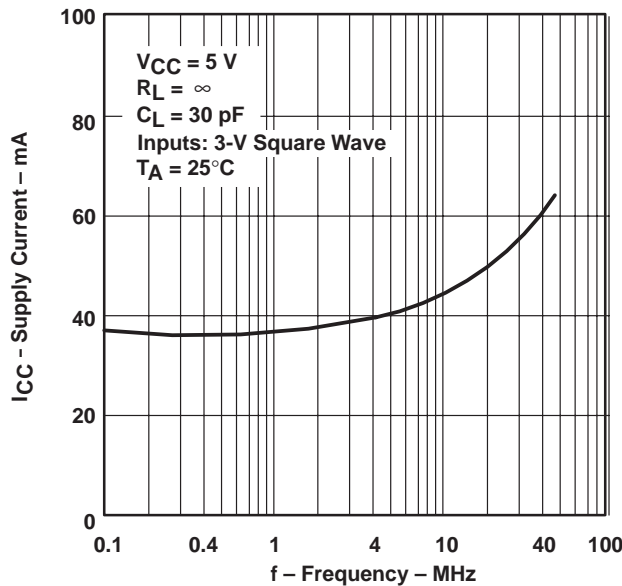


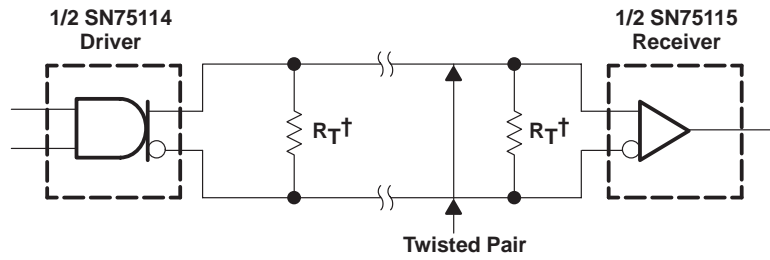
Figure 10

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. These parameters were measured with the active pullup connected to the sink output.

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APPLICATION INFORMATION



$^\dagger R_T = Z_0$. A capacitor can be connected in series with R_T to reduce power dissipation.

Figure 11. Basic Party-Line or Data-Bus Differential Data Transmission

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-88744022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88744022A SNJ55 114FK	Samples
5962-8874402EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874402EA SNJ55114J	Samples
5962-8874402FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874402FA SNJ55114W	Samples
JM38510/10403BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10403BEA	Samples
M38510/10403BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10403BEA	Samples
SN55114J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55114J	Samples
SN75114D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75114 9614CD	Samples
SN75114DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75114 9614CD	Samples
SN75114DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75114 9614CD	Samples
SN75114N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75114N	Samples
SN75114NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75114N	Samples
SNJ55114FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-88744022A SNJ55 114FK	Samples
SNJ55114J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874402EA SNJ55114J	Samples
SNJ55114W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8874402FA SNJ55114W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN55114, SN75114 :

● Catalog: [SN75114](#)

● Military: [SN55114](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK





- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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