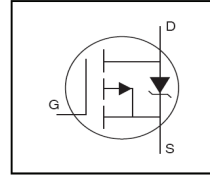
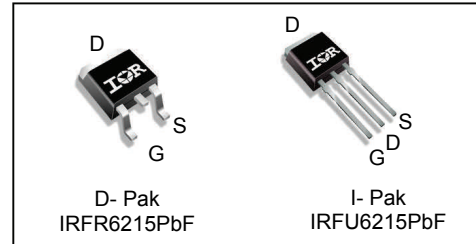


- P-Channel
- 175°C Operating Temperature
- Surface Mount (IRFR6215)
- Straight Lead (IRFU6215)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

HEXFET® Power MOSFET



V_{DSS}	-150V
$R_{DS(on)}$	0.295Ω
I_D	-13A



G	D	S
Gate	Drain	Source

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFU6215PbF	I-Pak	Tube	75	IRFU6215PbF
IRFR6215PbF	D-Pak	Tube	75	IRFR6215PbF
		Tape and Reel Left	3000	IRFR6215TRLpBf

Absolute Maximum Ratings

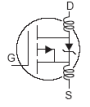
Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-13	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{V}$	-9.0	
I_{DM}	Pulsed Drain Current ①⑥	-44	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②⑥	310	mJ
I_{AR}	Avalanche Current ①⑥	-6.6	A
E_{AR}	Repetitive Avalanche Energy ①⑥	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T_{STG}			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ②	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-150	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.295	Ω	V _{GS} = -10V, I _D = -6.6A ④
		—	—	0.58		V _{GS} = -10V, I _D = -6.6A ④ T _J = 150°C
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
gfs	Forward Trans conductance	3.6	—	—	S	V _{DS} = -50V, I _D = -6.6A⑥
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -150V, V _{GS} = 0V
		—	—	-250		V _{DS} = -120V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	—	66	nC	I _D = -6.6A
Q _{gs}	Gate-to-Source Charge	—	—	8.1		V _{DS} = -120V
Q _{gd}	Gate-to-Drain Charge	—	—	35		V _{GS} = -10V, See Fig. 6 and 13 ④⑥
t _{d(on)}	Turn-On Delay Time	—	14	—		ns
t _r	Rise Time	—	36	—	I _D = -6.6A	
t _{d(off)}	Turn-Off Delay Time	—	53	—	R _G = 6.8Ω	
t _f	Fall Time	—	37	—	R _D = 12Ω, See Fig. 10 ④⑥	
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead ,6mm (0.25in.) from package and center of die contact⑤
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	860	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	220	—		V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance	—	130	—		f = 1.0MHz, See Fig. 5 ⑥


Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	-44		
V _{SD}	Diode Forward Voltage	—	—	-1.6	V	T _J = 25°C, I _S = -6.6A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	160	240	ns	T _J = 25°C, I _F = -6.6A
Q _{rr}	Reverse Recovery Charge	—	1.2	1.7	μC	di/dt = 100A/μs ④⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				


Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig.11)
- ② starting T_J = 25°C, L = 14mH, R_G = 25Ω, I_{AS} = -6.6A.(See Fig.12)
- ③ I_{SD} ≤ -6.6A, di/dt ≤ -620A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.
- ⑥ Uses IRF6215 data and test conditions.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

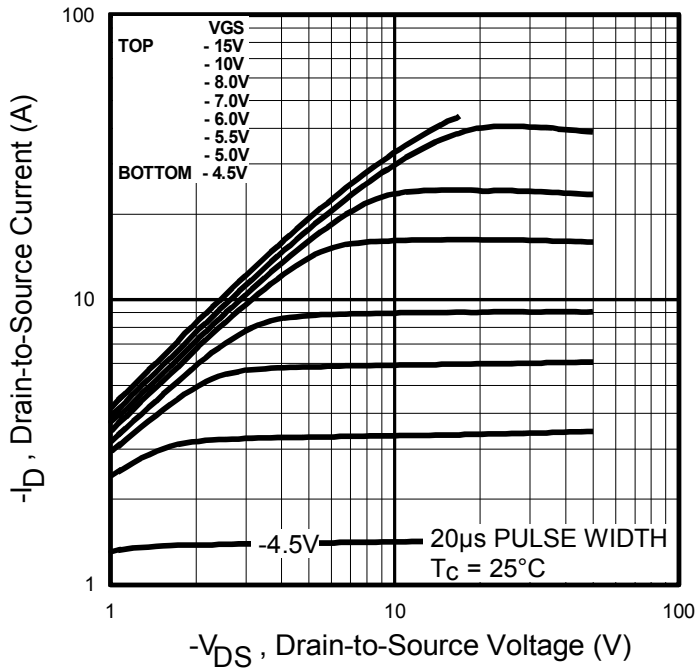


Fig. 1 Typical Output Characteristics

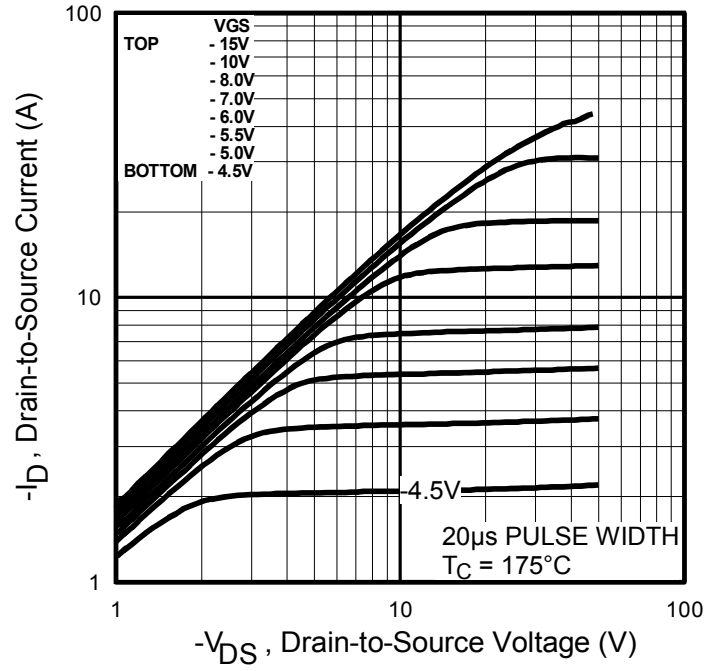


Fig. 2 Typical Output Characteristics

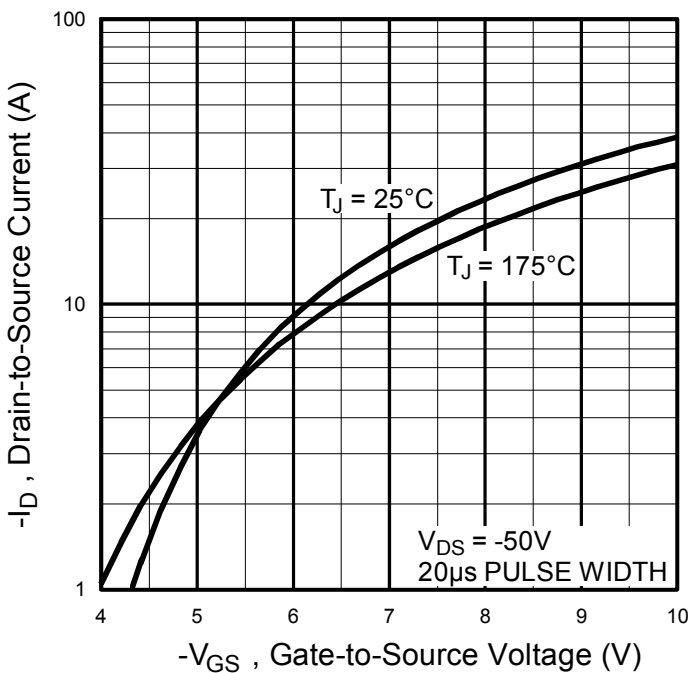


Fig. 3 Typical Transfer Characteristics

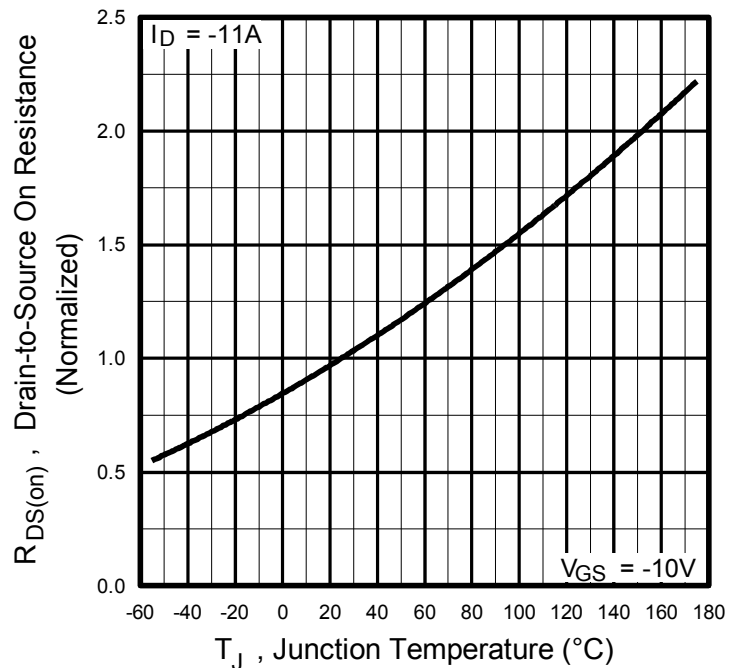


Fig. 4 Normalized On-Resistance vs. Temperature

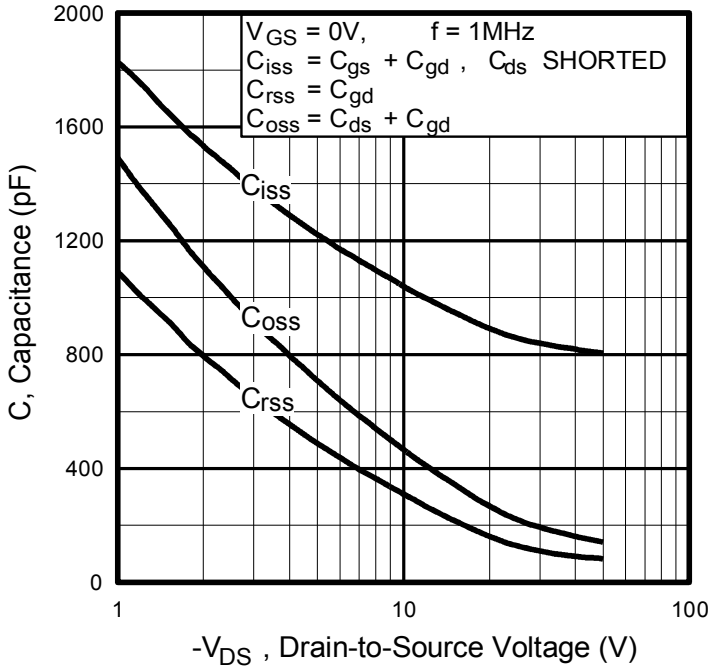


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

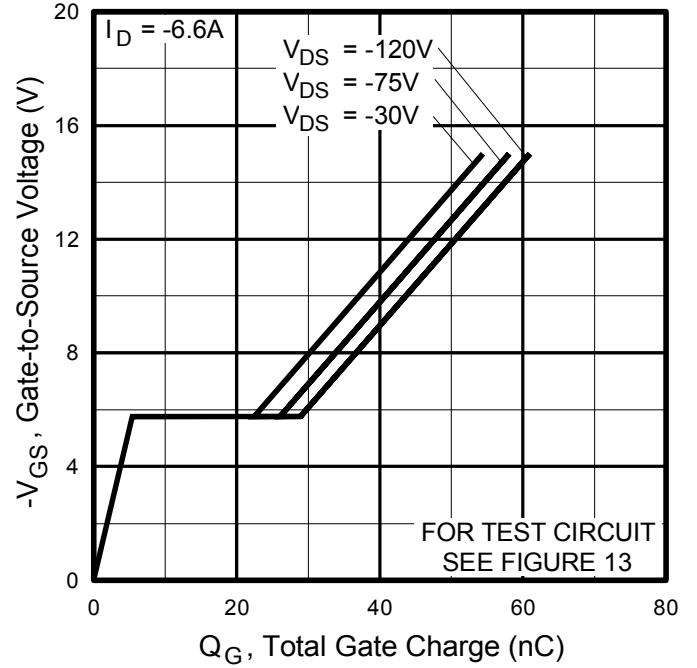


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

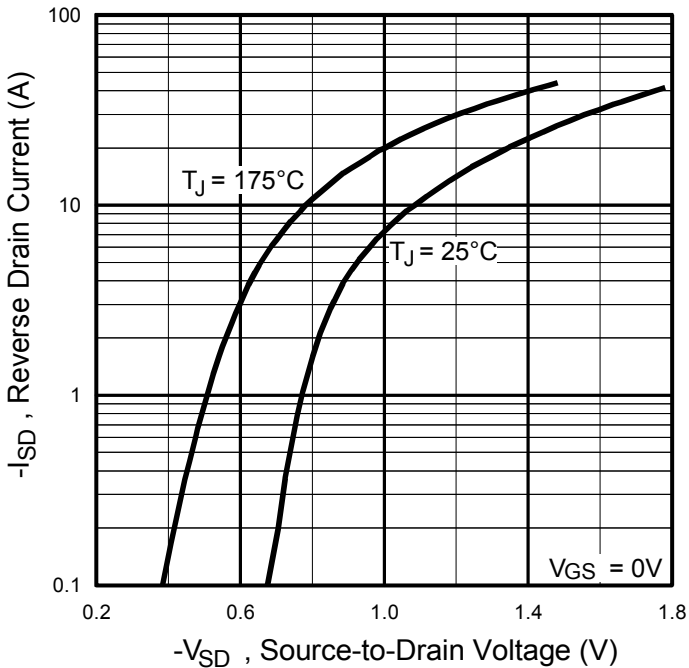


Fig 7. Typical Source-to-Drain Diode Forward Voltage

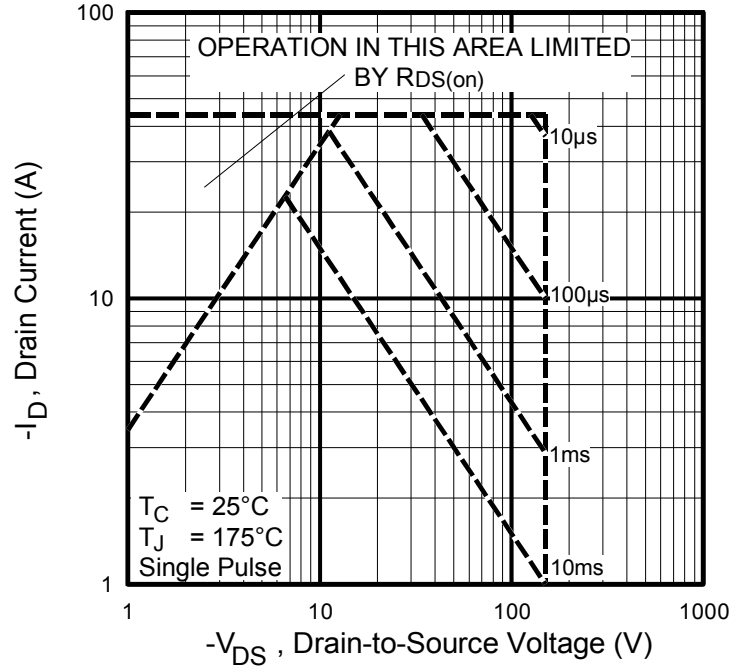


Fig 8. Maximum Safe Operating Area

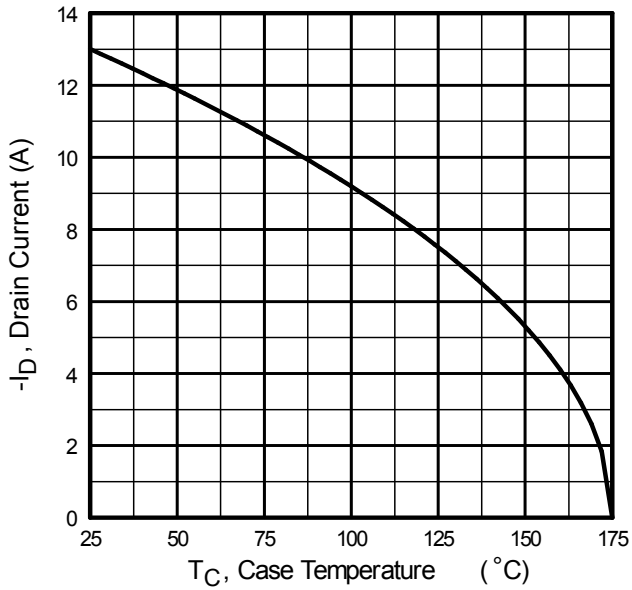


Fig 9. Maximum Drain Current vs. Case Temperature

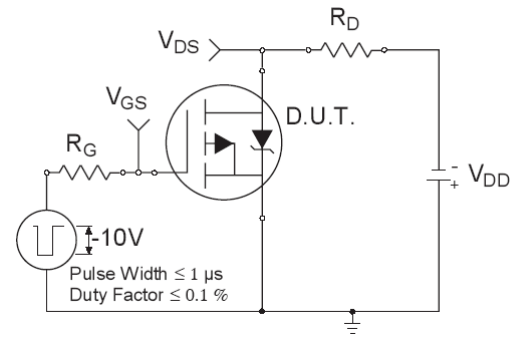


Fig 10a. Switching Time Test Circuit

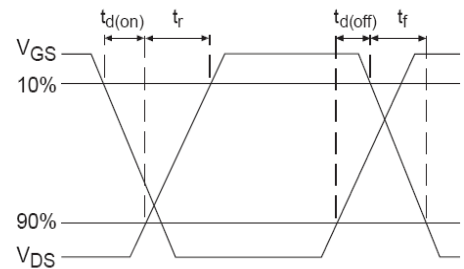


Fig 10b. Switching Time Waveforms

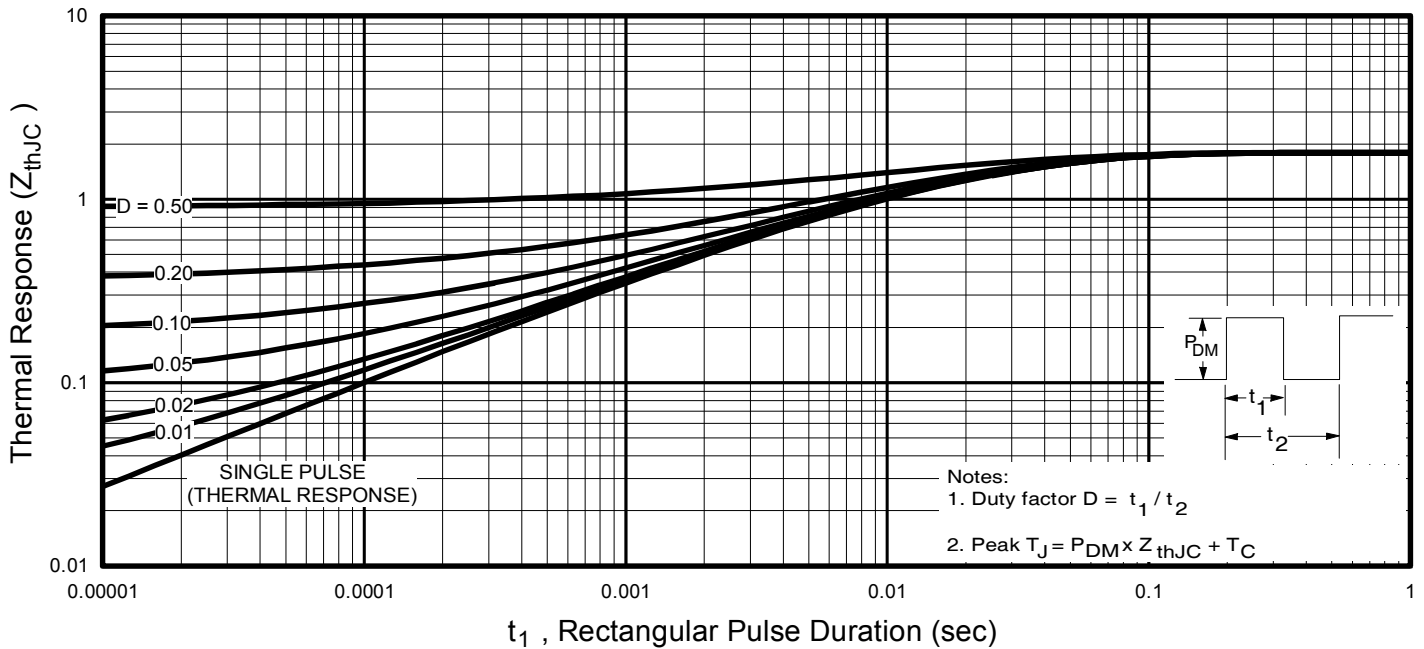


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

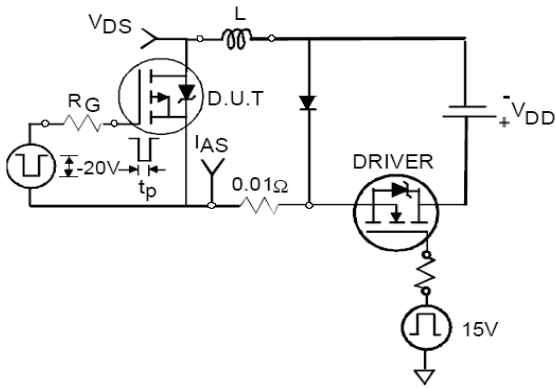


Fig 12a. Unclamped Inductive Test Circuit

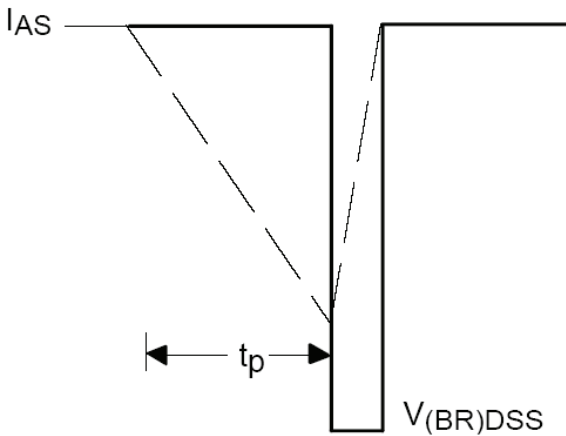


Fig 12b. Unclamped Inductive Waveforms

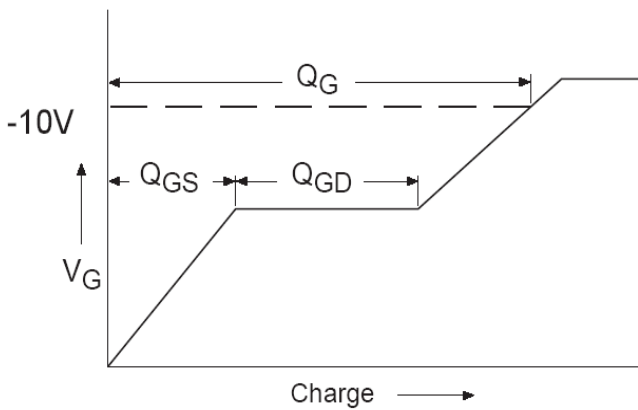


Fig 13a. Gate Charge Waveform

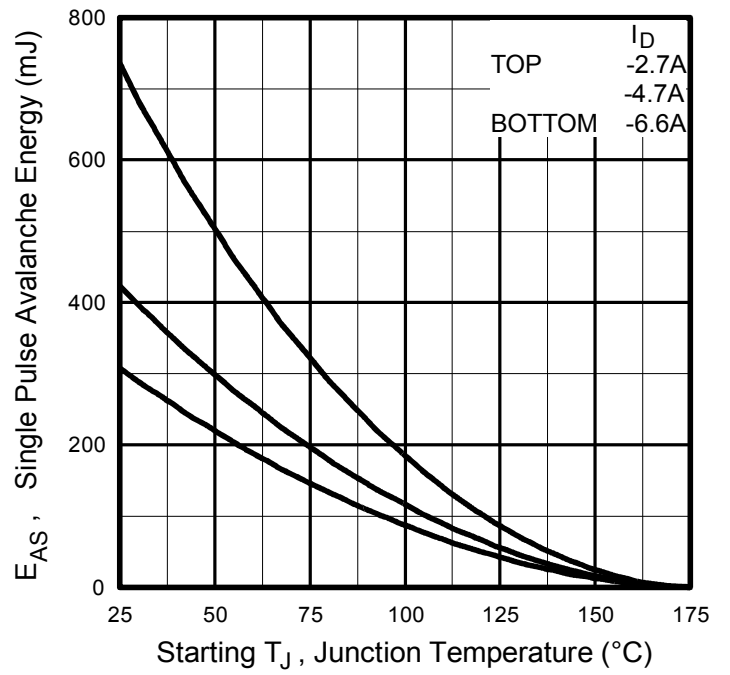


Fig 12c. Maximum Avalanche Energy vs. Drain Current

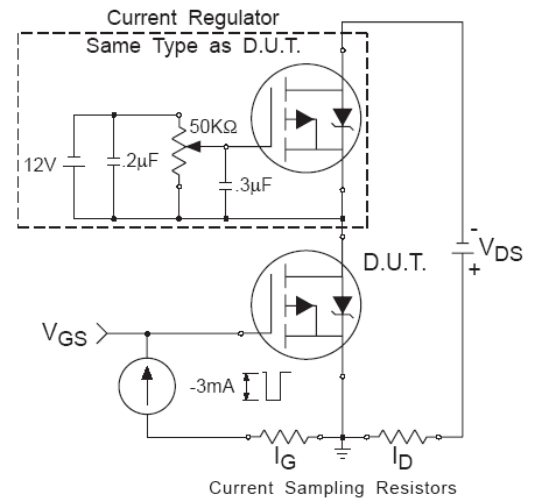
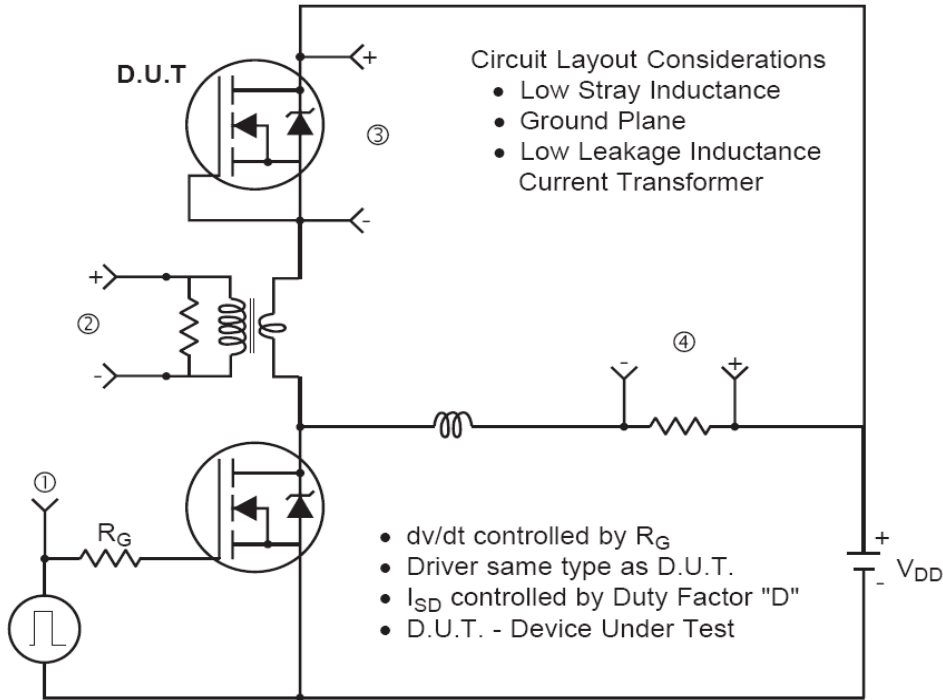
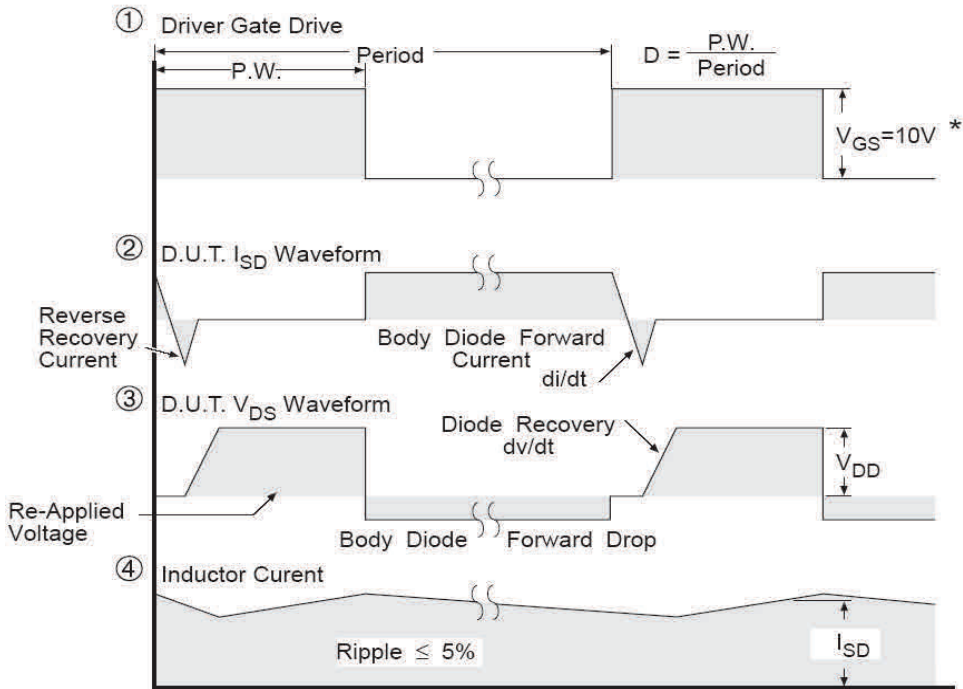


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



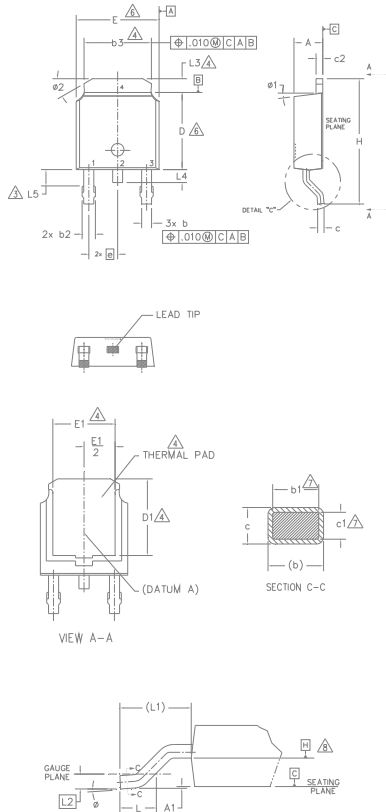
* Reverse Polarity of D.U.T for P-Channel



* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
 - △ LEAD DIMENSION UNCONTROLLED IN L5.
 - △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
 - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
 - △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
 - △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
 - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	2.18	2.39	.086	.094	7	
A1	-	0.13	-	.005		
b	0.64	0.89	.025	.035		
b1	0.64	0.79	.025	.031		
b2	0.76	1.14	.030	.045		
b3	4.95	5.46	.195	.215		4
c	0.46	0.61	.018	.024		7
c1	0.41	0.56	.016	.022		
c2	0.46	0.89	.018	.035		6
D	5.97	6.22	.235	.245		
D1	5.21	-	.205	-	4	
E	6.35	6.73	.250	.265	6	
E1	4.32	-	.170	-	4	
e	2.29 BSC		.090 BSC		LEAD ASSIGNMENTS	
H	9.40	10.41	.370	.410		
L	1.40	1.78	.055	.070		
L1	2.74 BSC		.108 REF.			
L2	0.51 BSC		.020 BSC		HEXFET	
L3	0.89	1.27	.035	.050		
L4	-	1.02	-	.040		
L5	1.14	1.52	.045	.060		
L6	0	10	0	10	IGBT & CoPAK	
L7	0	15	0	15		
L8	25	35	25	35		
L9	25	35	25	35		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

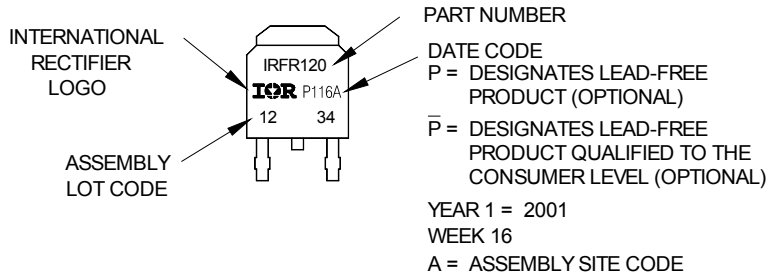
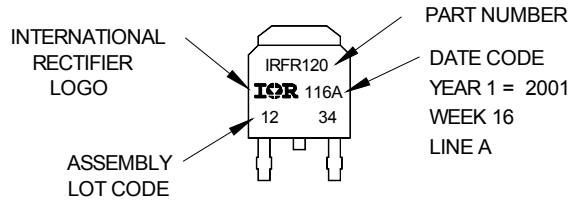
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON VV 16, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

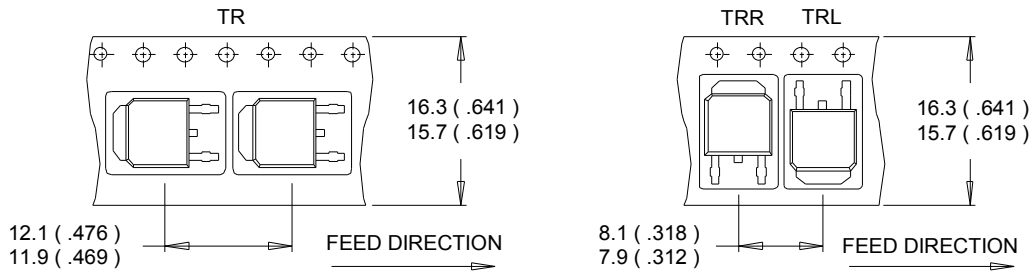
"P̄" in assembly line position indicates "Lead-Free" qualification to the consumer-level

OR

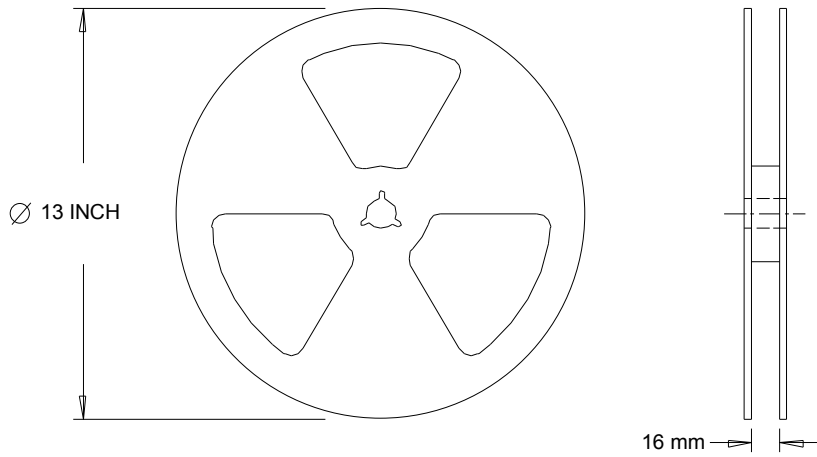


Note: For the most current drawing please refer to Infineon's web site www.infineon.com

D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to Infineon's web site www.infineon.com

Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F) ^{††}	
Moisture Sensitivity Level	D-Pak	MSL1 (per JEDEC J-STD-020D) ^{††}
	I-Pak	
RoHS Compliant	Yes	

† Qualification standards can be found at Infineon's web site www.infineon.com

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Comments
5/31/2016	<ul style="list-style-type: none"> Updated datasheet with corporate template. Added disclaimer on last page.

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Edition 2016-04-19

Published by

Infineon Technologies AG

81726 Munich, Germany

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